Exposure of PMMA with STM under Ambient Condition

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Abstract

The development of quantum electronics depends mainly on the development of nano-processing. STM has been a powerful tool for nano-processing. Before, the exposure of PMMA with STM could only be done in unltra high vacuum. The problem for exposure of PMMA under ambient condition is the unstability of the tip at tunnel condition. We used two measures to attack the problem:(1)adopted special procedure to prepare the W tip. After the formation of the tip, the tip was further etched for 1s;(2)first let the system go into tunnel condition at lower voltage then raised the voltage to exposure value gradually. After these two mwasures, the tip could be stablized under ambient condition. Afterwards, we used three set of labels to approach gradually from large area to small area to locate the exposure region. Finally, we have exposed 20nm thick of PMMA under ambient condition with STM and have obtained lines of 300nm linewidth.

1 Introduction

From the inception of integrated circuit, its integration scale has become larger and larger. The expansion of integration scale relies on the narrowing of feature line. According to the road map for development of integrated circuit by Semiconductor Industry Association of USA, by the first decade of 21st century, the line width of integrated circuit is going to reach <100nm magnitude. At that stage, the conventional method of optical lithography that has been used till now can not be competent anymore. Now research laboratories are searching ways to reach sub-100 nm goal. X-ray lithography, electron beam lithography and STM nanoprocessing have been the focus of many research laboratories.

The number of laboratories conducting STM research has been numurous. STM is a powerful tool for nanoprocessing. It has many ways for nanoprocessing. For example, direct lithography on substrate, tip induced chemical vapor deposition, exposure of electron beam resist, ect.. Among them, exposure of electron beam resist has special significance. It can transfer its pattern onto various substrates.

Since electron beam resist is an insulator. Exposure of electron beam resist with STM has its special difficulties. Before, exposure of electron beam resist PMMA could only be done under ultra high vacuum conditions, there was electrical breakdown under ambient conditions[1]. We have modified some of the experimental conditions and succeeded in exposure of PMMA with STM under ambient conditions.

2 Experimental and results

Our STM was purchased from Benyuan Company, Institute of Chemistry, Chinese Academy of Sciences. It operates under ambient conditions.

Exposure of PMMA needs about 30V bias voltage. Our STM can only bear 12V bias voltage. A 28 mega Ohm resistor was connected in series with STM preamplifier to reduce the voltage applied to the preamplifier so that it bears no more than 12V voltage.

Exposure of PMMA needs very flat substrate surface. We used Si waffer as substrate material for PMMA resist. Since Si waffer is usually coated with a layer of SiO_2, preventing its conductivity, we sputtered

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500 angstrom Au on top of the waffer to insure smoothness and conductivity.

0.75% PMMA dissolved in chlorobenzene was spaned on substrate with 8000 revolution/min for 20s. Then, it was baked for 2 hours at 180^0C. The thickness of PMMA was determined as about 20nm with stylus stepper. Since STM requires conductive substrate, the thickness of PMMA must be relative thin, from 20nm to 50nm[1].

We have adopted two measures to solve the problem of electrical breakdown.

First we have built an electrical apparatus to etch the W tip. When the tip is formed, it can cut off the electrical supply and stop etching process automatically. We have found that when the etching process is stopped immediately after the formation of the tip, the tip is usually crash when approaching the tunneling state or during the experiment. We add a delay mechanism to the apparatus and etch the tip further for 0.5s or 1s after its formation. The tip thus prepared do not crash when used properly. Analyzing the reason, we believe that thus prepared tip have larger shaft and better protrusions on the top of the apex[2].

Second, we also found that when the tip approaching the PMMA surface to form field emission state with -23V bias voltage, the tip was very easy to be damaged. What we did was to approach the tip to the PMMA suface at bias voltage -4V to set up the tunneling state. After that , raise the bias voltage to -23V. In this way, the electrical breakdown was avoided at lower voltage.

Exposure conditions were -23V (tip negative), 80pA. Scan speed was 0.5 micrometer/s. At this bias voltage, the tip works at filed emission regime. Since PMMA is an insulator, a lower tunneling current should be used. But due to the limitation of the sensitivity of our STM, 80 pA is the lowest tunneling current we could use.

Exposure manner was to scan STM tip while the tip and the substrate was under field emssion condition. Exposure pattern was generated by a home-made software.

After the exposure, the exposed PMMA pattern (positive resist) needs to be developed. The developer used was 1:3 isopropyl alchol : 4-methyl-2-pentanone. We determined the developing time this way:(1)make a scratch with a knife on 20 nm thick PMMA on Si waffer. Then dip the waffer into the developer to determine how fast the PMMA dissolve into the developer. The scratch disapper in about 80s, i.e., 20nm thick PMMA dissolved into the developer; (2) expose a whole area instead separate lines to observe the Au surface with Scanning Electron Microscope (SEM). In this way, we determined that 8s as optimum developing time.

There was another problem need to be solved. After exposure and development, the exposure pattern needs to be imaged by SEM. This is a difficult task. Try to imagine the exposure region only 2 micrometer X 2 micrometer square on the 0.5 cm X 0.5 cm square substrate. The linear ratio is 2500 times and the area ratio is 6,250,000 times. To locate such a small area in such a substrate is not easy. We adopted three coordinate system to attack this problem. First, make a mm wide long line near STM tip region. Second, after exposure, retract the ceramics of STM, then crash the tip right at the exposure region. After the crash, use the STM tip to scratch a thin line (about 1 micrometer in linewidth). Thirdly, at the end of the line crash the tip into a mm spot. When taking SEM picture, first locate the mm wide long line on the substrate. Around this line, looking for the mm scratch spot. From this spot, along the scratched micrometer line, look for the exposed region.

Before taking SEM picture, a 50 angstrom Au film was deposited onto the sample to prevent the charging effect.

Figure 1 is a SEM picure of STM exposed PMMA under ambient condition. The exposure conditions are

as follows: bias voltage -23V, field emission current 80pA, scan speed 0.5 micrometer/s, and the tip was further etched for 1s after its formation. The minimum line width is 300nm. The obtained line width is a little bit larger compared with ultra high vacuum case. This may be due to the high level of noise for PMMA sample at ambient condition.

Efforts has been made to reduce the line width but has not been successful yet.

3 Conclusion

We have succeeded in exposing 20nm thick PMMA with STM under ambient condition and obtained 300nm PMMA lithographic lines.

References

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