Improvement in the electrical performance and bias-stress stability of dual-active-layered silicon zinc oxide/zinc oxide thin-film transistor*

Yu-Rong Liu(刘玉荣)[1,2,†], Gao-Wei Zhao(赵高位)[1], Pai-To Lai(黎沛涛)[3], and Ruo-He Yao(姚若河)[1,2]

[1] *The School of Electronic and Information Engineering, South China University of Technology, Guangzhou* 510640, *China*
[2] *National Engineering Technology Research Center for Mobile Ultrasonic Detection, South China University of Technology, Guangzhou* 510640, *China*
[3] *Department of Electrical and Electronic Engineering, the University of Hong Kong, Pokfulam Rd., Hong Kong, China*

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Si-doped zinc oxide (SZO) thin films are deposited by using a co-sputtering method, and used as the channel active layers of ZnO-based TFTs with single and dual active layer structures. The effects of silicon content on the optical transmittance of the SZO thin film and electrical properties of the SZO TFT are investigated. Moreover, the electrical performances and bias-stress stabilities of the single- and dual-active-layer TFTs are investigated and compared to reveal the effects of the Si doping and dual-active-layer structure. The average transmittances of all the SZO films are about 90% in the visible light region of 400 nm–800 nm, and the optical band gap of the SZO film gradually increases with increasing Si content. The Si-doping can effectively suppress the grain growth of ZnO, revealed by atomic force microscope analysis. Compared with that of the undoped ZnO TFT, the off-state current of the SZO TFT is reduced by more than two orders of magnitude and it is 1.5×10^{-12} A, and thus the on/off current ratio is increased by more than two orders of magnitude. In summary, the SZO/ZnO TFT with dual-active-layer structure exhibits a high on/off current ratio of 4.0×10^{6} and superior stability under gate-bias and drain-bias stress.

Keywords: thin film transistor (TFT), silicon-doped zinc oxide, dual-active-layer structure, bias-stress stability

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1. Introduction

Zinc oxide (ZnO)-based semiconductors that are used as active channel layers for thin film transistors (TFTs) have recently attracted a great deal of attention due to their advantages such as high field-effect mobilities, good uniformities, high transparencies in the visible light range, compatibility with the conventional a-Si TFT fabrication process, and low-temperature deposition process used for flexible electronics.[1–3] These excellent characteristics could meet the requirements for faster switching speed, lower power consumption and higher resolution for next-generation active-matrix liquid-crystal displays (AMLCDs) and active-matrix organic light-emitting diode (AMOLED) displays. Over the past two decades, most of the high-performance ZnO-based TFTs are based on indium-incorporated oxide semiconductors, e.g., indium zinc oxide (IZO),[4] indium zinc tin oxide (IZTO),[5] indium hafnium zinc oxide (IHZO),[6] and indium gallium zinc oxide (IGZO).[7] However, indium is relatively rare in Earth's crust, which makes those technologies easily subject to a material shortage. Some researchers have recently reported some new oxide semiconductors free of indium, which may be used as alternative channel materials for oxide TFTs, including aluminum zinc tin oxide (AZTO),[8] zinc tin oxide (ZnSnO),[9] and silicon zinc oxide (SZO).[10] Among these elements, silicon (Si) is an abundant element in the Earth, and an appropriate Si content in ZnO-based film can not only achieve stable and dense films, but also suppress the formation of oxygen vacancies efficiently, due to its high oxygen bonding ability.[11] In addition, a dual-active-layer structure was adopted to achieve both better electrical performance and bias stability by combining two semiconducting thin film channel layers having different compositions.[12–14] In this work, active single and bilayer structure TFT with silicon-doped ZnO (SZO) thin film employed as the channel layer are fabricated by using a co-sputtering method. Effects of silicon content on optical transmittance of the SZO thin film and electrical properties of the SZO-TFT are investigated. Moreover, the electrical performances and bias stabilities of the single- and dual-active-layer TFTs are investigated and compared to reveal the effects of Si doping and dual-active-layer structure.

2. Experimental details

The schematic TFT structure is shown in Fig. 1. To fabricate the devices with the most commonly-used bottom-gate top-contact structures, 150-nm SiO_2 was thermally grown as the gate dielectric layer on the top of a heavily-doped n-type Si wafer, which acted as both the substrate and gate contact. Three different types of active layer configurations were em-

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†Corresponding author. E-mail: phlyr@scut.edu.cn

ployed for the TFTs. The first one consisted of a single ZnO layer, and the second one had a single layer of SZO with different Si contents, each with a nominal thickness of 30 nm, as illustrated in Fig. 1(a). The last type was a bilayer active stack comprised of a ZnO film (nominal thickness of 15 nm grown directly on the gate dielectric) with a layer of SZO film (nominal thickness of 15 nm) on the top of the ZnO film as shown in Fig. 1(b). The individual active layers were deposited by sputtering at a base pressure of 5×10^{-4} Pa. The ZnO films were deposited by DC sputtering a ZnO target (99.995%, purity) at a substrate temperature of 350 °C. During the sputtering, the mixing gas ratio of O_2/Ar was 1 with a working pressure of 1 Pa, and the DC power was 30 W. The SZO films were deposited by using a co-sputtering method with ZnO target (99.995%, purity) and intrinsic Si target (99.998%, purity). The co-sputtering process was carried out at a substrate temperature of 150 °C. The mixing gas ratio of O_2/Ar was 1/3 with a working pressure of 1 Pa. The DC power applied to the ZnO target was 30 W, and the radio-frequency (RF) powers applied to the Si target were 20 W, 30 W, and 60 W, respectively, so as to vary the Si content of the SZO thin film. After the active layer was deposited, aluminum was thermally evaporated through a shadow mask to form the source/drain (S/D) electrodes of the transistors. The channel width (W) and length (L) of the device on the mask were 600 μm and 50 μm, respectively.

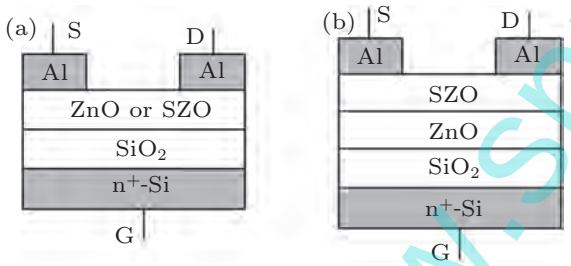

Fig. 1. Schematic diagram of TFT devices preparing (a) ZnO or SZO thin film as a single active layer, (b) SZO/ZnO thin film as a double active layer.

The thickness values of the silicon oxide and active layers were measured by spectroscopic reflectometer (Ocean Optics, NanoCalc-2000). The optical transmittancies of the SZO and ZnO films were measured by using a UV/visible spectroscope (Agilent, Cary 60). The values of electrical resistivity (ρ) of the films were measured by using a four-point probe resistivity measurement system (Four Probes Tech., RTS-9) and the results are shown in Table 1. X-ray photoelectron spectroscopy (XPS) measurements were performed to analyze the relative Si content distributed in the SZO film by using Cu-Ka radiation (Bruker, D8 Advance diffractometer). The atomic percentages of Si in the SZO film were calculated to be 2.3%, 3.8%, and 7.9% for the RF powers of 20 W, 30 W, and 60 W respectively. The structural properties of the SZO films were investigated by using an atomic force microscope (AFM) (Ben Yuan CSPM 4000 SPM). The electrical characterizations and stabilities of the TFTs were performed at room temperature in the dark by using a semiconductor parameter analyzer (Agilent 4156C).

3. Results and discussion

In order to analyze the optical transmittancies of the SZO thin films with different Si content in the visible light range, the ZnO and SZO films are deposited on the top of a glass slide. Figure 2 shows the variations of optical transmittance with wavelength of the SZO films in the UV-to-visible range. The average transmittance of the SZO films is about 90% in the visible light region of 400 nm–800 nm, and higher than that of the undoped ZnO film, indicating that SZO film is more suitable for applications in transparent electronic devices. In addition, the near-band-edge wavelength, at which light transmittance starts to occur, is approximately 380 nm for the ZnO film without Si. As the Si incorporated into the ZnO film increases, a blue shift of the absorption region edge can be observed, indicating that the optical band gap (E_g) of the SZO film also gradually increases with the increase of Si content. The optical band gap of the SZO film can be calculated from Fig. 2 from the following formula[15]

$$E_g = \frac{hc}{\lambda_c} = \frac{1.24}{\lambda_c}, \tag{1}$$

where λ_c (in unit μm) is the long-wavelength cutoff of the absorption edge of the SZO film, corresponding to the band gap E_g of the semiconductor, and the results are shown in the inset of Fig. 2. For the ZnO film without Si, the optical band gap is 3.29 eV, but increases to 3.86 eV for the SZO film with 7.9% Si content.

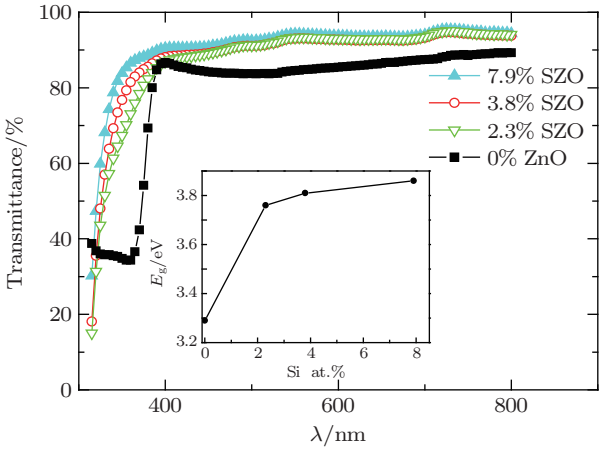

Fig. 2. (color online) Optical transmission spectra of the SZO thin films with different Si contents. The inset shows the direct optical band gaps of the SZO films.

Figures 3(a)–3(c) show the AFM images of the SZO thin films for 2.3%, 3.8%, and 7.9% Si content, respectively. It can be seen that the SZO film shows a clear polycrystalline structure at low Si content, and an inferior polycrystalline characteristic for high Si content. The grain size of the SZO films are about 85 nm, 40 nm, and 20 nm for the 2.3%, 3.8%, and 7.9%

Si content, respectively, indicating that the Si-doping can effectively suppress the grain growth of ZnO. In addition, the RMS roughness values of the SZO films are about 13.4 nm, 9.3 nm, and 6.1 nm for the 2.3%, 3.8%, and 7.9% Si content by three-dimensional (3D) analysis of Figs. 3(a)–3(c), respectively.

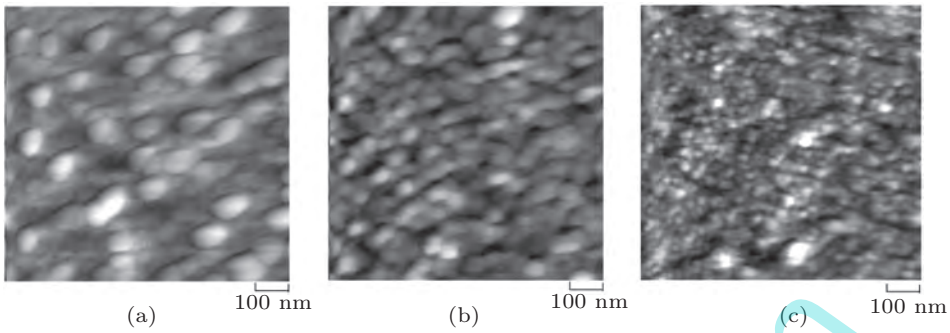

Fig. 3. AFM images of the SZO thin films for Si content values of (a) 2.3%, (b) 3.8%, and (c) 7.9%.

Figure 4(a) shows the output characteristics of a Si-doped ZnO TFT, which exhibits clear current saturation. The transistor has good ohmic contact at the Al/channel interface because no current crowding at low V_{DS} is found. Figure 4(b) shows the transfer curves of the SZO TFTs (at a drain-source voltage V_{DS} of 30 V), which exhibit quite different electrical properties depending on the Si content. The on-state current largely decreases with increasing Si content in the SZO thin film, but the off-state current presents a dramatic decrease when a small amount of silicon is added in the ZnO active layer. The threshold voltage (V_{th}) and field effect mobility (μ_{FE}) are calculated from the curve of drain current $(I_D)^{1/2}$ versus V_{GS} (gate bias) by the following equation:

$$I_D = \frac{W}{2L}\mu_{FE}C_i(V_{GS} - V_{th})^2, \tag{2}$$

where C_i is the capacitance per unit area of the gate insulator. The subthreshold swing (SS), defined as the necessary V_{GS} to increase I_D by one decade, is calculated by

$$SS = \left(\frac{d\log(I_D)}{dV_{GS}}\right)^{-1}. \tag{3}$$

Therefore, the electrical parameters of the SZO TFTs can be readily extracted from the transfer curves and summarized in Table 1. The undoped ZnO TFT shows a relatively high field-effect mobility (~ 1.06 cm^2/V·s), but the off-state current is large (~ 0.66 nA) and thus a low on/off current ratio ($\sim 1.0\times10^5$), which is too low for application in active-matrix flat-panel displays. Compared with that of the undoped ZnO TFT, the threshold voltage of the SZO TFT shifts towards the negative direction with increasing Si content and the off-state current is reduced by more than two orders of magnitude with a minimum of 1.5 pA for 2.3% Si content. However, the field-effect mobility of the SZO TFT decreases monotonically from 1.06 cm^2/V·s to 1.5×10^{-4} cm^2/V·s with increasing Si content, leading to a decrease of the on-state current. Therefore, only a very small amount of Si can increase the on/off current ratio, e.g., for the SZO TFT with 2.3% Si content, the on/off current ratio is increased by more than two orders of magnitude and reaches up to 7.9×10^6. The decrease in the off-state current is related to the resistivity of the SZO film gradually increasing with the augment of Si content. The field-effect mobility decrease of the SZO TFT can be explained as follows. First, the bandgap increase of the SZO film caused by Si doping results in a reduction of energy band width which leads to the increase of electron effective mass, and thus lowering the electron mobility. Second, the grain size of the ZnO film decreases with increasing Si content, resulting in the decrease of carrier mobility. Third, the decrease of carrier mobility is attributed to the low carrier concentration caused by Si acting as a carrier suppressor in the film and carrier scattering effect of the Si doping. This is because during the SZO film deposition, the Si and O in the plasma state can easily combine with each other due to the relatively high bond strength of Si–O (799.6 kJ/mol) compared with Zn–O (395 kJ/mol).[11]

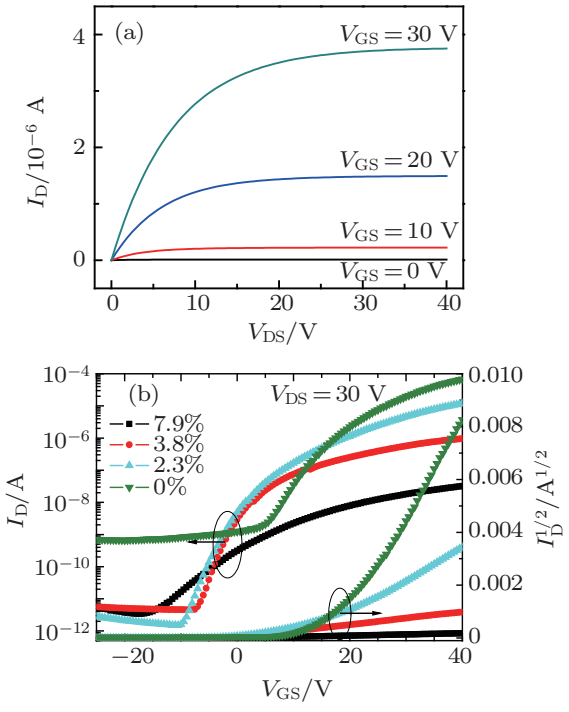

Fig. 4. (color online) (a) Output characteristics of the SZO TFT with 2.3% Si content, (b) transfer characteristics of the SZO-TFTs with different Si content at V_{DS}=30 V.

Table 1. Main performance parameters of the SZO-TFTs with different Si content for single active layer and the SZO/ZnO TFT for double active layer.

Active layer	ρ/Ω·cm	I_{off} /A	I_{on}/I_{off}	V_{th}/V	SS/V·Dec^{-1}	μ/cm^2·V^{-1}·s^{-1}
7.9% SZO	6.1×10^{4}	3.4×10^{-12}	9.4×10^{3}	1.2	6.8	1.5×10^{-4}
3.8% SZO	5.8×10^{2}	4.6×10^{-12}	2.1×10^{5}	1.5	2.3	3.8×10^{-3}
2.3% SZO	40.5	1.5×10^{-12}	7.9×10^{6}	13.5	2.2	0.12
No-doped ZnO	2.4	6.6×10^{-10}	1.0×10^{5}	18.4	3.5	1.06
SZO/ZnO		1.3×10^{-11}	4.0×10^{6}	18.5	2.6	1.02

In order to suppress the reductions of carrier mobility and on-state current caused by Si doping in the single-layered SZO TFT, an SZO/ZnO TFT with a double-active-layer structure as shown in Fig. 1(b) is fabricated. The top layer is SZO thin film with 2.3% Si content, and the bottom layer is undoped ZnO thin film. Figure 5 shows the transfer characteristics of the SZO/ZnO TFT at a drain bias of 30 V, together with those of ZnO TFF and SZO TFT for comparison purposes. The electrical parameters can be extracted from Fig. 5 and summarized in Table 1.

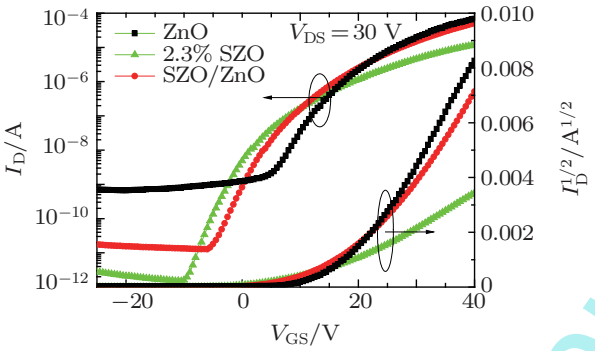

Fig. 5. (color online) Transfer characteristics of ZnO-based TFTs with single- and dual-active-layer structures at V_{DS} = 30 V.

Among the three types of active layer structures, the SZO/ZnO TFT exhibits the best device performance. Compared with that of the 2.3% SZO TFT, although the off-state current of the SZO/ZnO TFT increases by one order of magnitude, the carrier mobility and on-state current both increase by one order of magnitude, and thus the on/off current ratio remains relatively high (at 4.0×10^{6}). Compared with that of ZnO TFT, the off-state current of the SZO/ZnO TFT decreases from 0.66 nA to 13 pA, and thus the on/off current ratio increases 40 times. Moreover, there is no reduction in the carrier mobility. Therefore, the SZO/ZnO dual-active-layer structure can achieve significant improvements in low-power operation and current-drive capability. Lower off-state current in the SZO/ZnO TFT with no reduction in carrier mobility can be explained as follows. A homojunction is formed between the SZO and ZnO layers due to their different energy bandgap structures, and thus forming an energy barrier at the SZO/ZnO interface for suppressing the off-state current. In addition, since the ionic potential of Si^{4+} is higher than that of Zn^{2+},[16] silicon oxide is formed more easily than zinc oxide in the sputtering process to suppress the oxygen vacancy and charge carrier, thus resulting in less oxygen vacancy and denser structure in the SZO film than in the ZnO film. Therefore, in the SZO/ZnO structure, the top SZO film can effectively protect the bottom ZnO channel from being influenced by the oxygen and water vapor in the air.

The electrical stabilities of the TFTs with single- and double-active layer structures are examined under positive gate-bias stress (PBS) and positive drain-bias stress (DBS), respectively. A gate bias V_{GS} of 20 V is applied to the gate electrode, with the source and drain electrodes connected to the ground (0 V) during the PBS, while a drain-bias V_{DS} of 20 V is applied to the drain electrode, with the source and gate electrodes grounded during the DBS. Figure 6 shows the evolutions of transfer characteristics for the ZnO-based TFTs with single- and double-active layer structures at a drain bias of 30 V after being subjected to a positive gate-bias voltage of 20 V for different stress times at room temperature. It can be observed that for the three kinds of active layer structures, there is a shift in the transfer curve in the positive direction. The off-state current decreases with increasing stress time because the defect states in the channel occupied by electrons during stressing (which do not emit immediately after stressing) cause a reduction in effective defect states. In addition, the SS and carrier mobility remain basically unchanged after the transistor has undergone the gate-bias stressing. It has been reported that the positive shift in V_{th} during the PBS can be explained by using a simple charge trapping or defect creation model.[17–19] Here, the SS value is not significantly affected during the PBS. This result suggests that charge trapping in the gate dielectric is more dominant than the creation of defects in the TFT.[17,20] However, it is worth mentioning that the bilayer-structure SZO/ZnO TFT shows better gate-bias stress stability with smaller threshold voltage shift (ΔV_{th}) (+1.07 V) than the single-layer-structure SZO TFT (+5.1 V) and ZnO TFT (+5.06 V) after being stressed for 120 min. The superior stability of the bilayer-structure SZO/ZnO TFT could be attributed to not only the reduction of trap sites by the passivation of the porous ZnO thin film due to the SZO layer, but also the formation of the interface between the ZnO and SZO layers. Previous researches have reported that such an interface with the captured free electrons contributes to a weakened electric field under gate-voltage stress.[21,22] Therefore, the bilayer structure SZO/ZnO TFT has a good stability under the PBS due to reduced interaction between the exposed back surface and the oxygen in ambient atmosphere, as well as the reduction of trap sites.

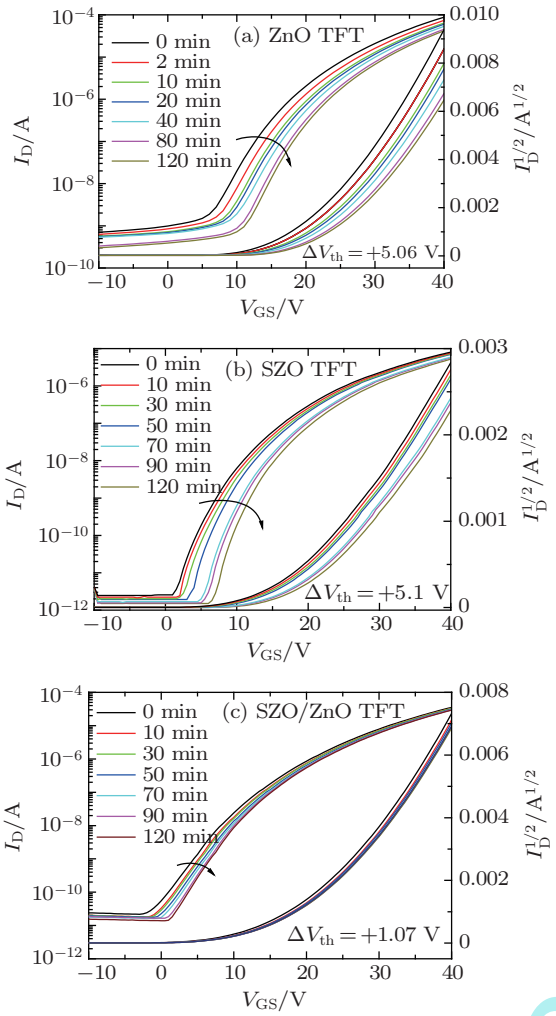

Fig. 6. (color online) Transfer characteristics of the ZnO-based TFTs with single- and dual-active-layer structures at $V_{DS} = 30$ V under a gate-bias stress of 20 V. Panel (a) is for the single-layered ZnO structure, panel (b) the single-layered SZO structure, and panel (c) the double-layered SZO/ZnO structure.

Figure 7 shows the variations of transfer characteristics of the ZnO-based TFTs for single- and double-active-layer structures at a drain bias of 30 V after being subjected to a drain-bias voltage of 20 V for different stress times at room temperature. Obviously, for the three kinds of active layer structures, the transfer curves shift toward the negative direction with increasing stress time, and the off-state currents increase slightly with increasing stress time. Similarly, the SS and carrier mobility are almost unchanged with increasing stress duration, indicating that the creation of defect states at the semiconductor/dielectric interface is not significant. However, the bilayer structure SZO/ZnO TFT shows better drain-bias stress stability with smaller threshold voltage shift (ΔV_{th}) (−1.60 V) than the single-layer structure SZO TFT (−6.33 V) and ZnO TFT (−5.5 V) after being stressed for 120 min. The negative Vth shift under the DBS can be explained below. Under the DBS, the lateral electric field near the drain depletion region is so high that electrons accelerated near the drain depletion region collide with and ionize the neutral deep donors such as oxygen vacancies, which are considered to exist abundantly in the active layer.[23] The positively ionized oxygen vacancies (Vo^{2+}) near the drain side can remain after the DBS because they are located above the conduction-band bottom,[24] and thus electrons in the active layer accumulate there for the conservation of charge neutrality. However, in the bilayer structure SZO/ZnO TFT, the higher-resistivity SZO layer and the energy barrier at the SZO/ZnO interface can reduce the lateral electric field caused by the DBS, and thus lowering the possibility of the Vo^{2+} generation and reducing the electron accumulation in the active layer. Therefore, the bilayer structure SZO/ZnO TFT displays better stability than the single-layer structure SZO TFT and ZnO TFT under the DBS. In addition, it is possible that the SZO film with less oxygen vacancy and denser structure can effectively block the oxygen and water vapor in the air because the H_2O adsorption at the back channel of TFT may induce an electron accumulation layer below the active surface,[25] and thus accelerating the device degradation under the DBS. However, further investigations are needed to probe the physical mechanism.

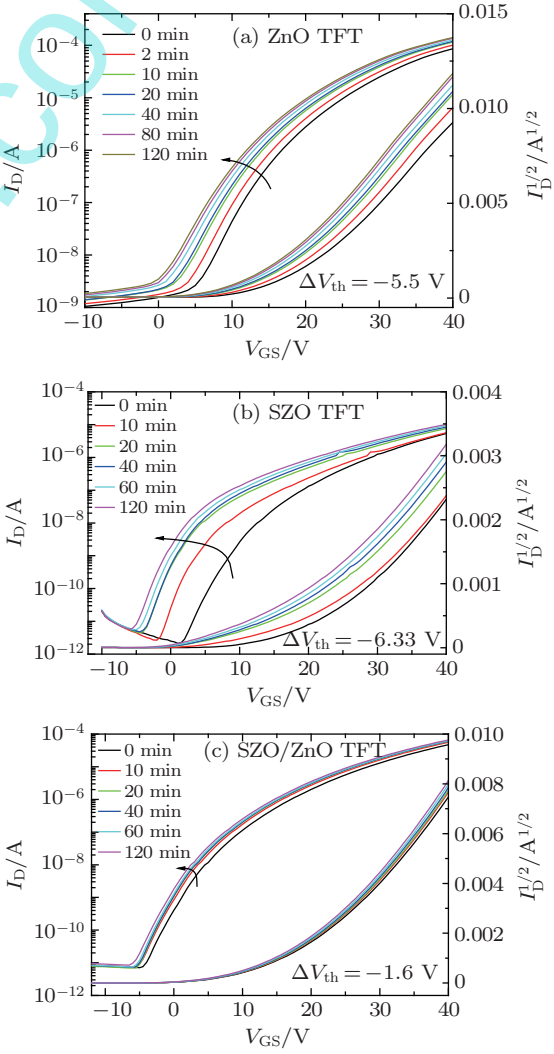

Fig. 7. (color online) Transfer characteristics of the ZnO-based TFTs with single- and dual-active-layer structures at $V_{DS} = 30$ V under a drain-bias stress of 20 V. Panel (a) is for the single-layered ZnO structure, panel (b) the single-layered SZO structure, and panel (c) the double-layered SZO/ZnO structure.

4. Conclusions

Active single- and bilayer structure thin-film transistors (TFTs) with Si-doped zinc oxide (SZO) and undoped zinc oxide (ZnO) thin film layers are fabricated by using a co-sputtering method. The doping of Si in the ZnO TFT reduces effectively the off-state current by more than two orders of magnitude and increases the on/off current ratio by more than two orders of magnitude due to the decrease of carrier concentration in the active channel layer, although the mobility is degraded. Compared with the active single-layer structure TFT with SZO and ZnO thin film, the active bilayer structure TFT with the combination of SZO and ZnO thin film layers exhibits a better electrical performance with both high on/off current ratio and high carrier mobility. On the other hand, the active bilayer structure TFT also shows a superior stability under gate- and drain-bias stresses, which is suitable for its application to AMLCD and AMOLED backplanes.

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