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High-κ organometallic lanthanide complex as gate dielectric layer for low-voltage, high-performance organic thin-film transistors

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ABSTRACT

Low-voltage pentacene-based organic thin-film transistors (OTFTs) have been fabricated using the high-κ organometallic lanthanide complex, $Tb(tta)_3L_{2NR}$ (tta = 2-thenoyltrifluoroacetonate, L_{2NR} = (−)-4, 5-pinene bipyridine) as the gate dielectric material. The optimized gate insulator exhibits a low leakage current density of $<10^{-7}$ A cm^{-2} under bias voltage of −5 V, a smooth surface with RMS of about 0.40 nm, a high capacitance of 43 nF cm^{-2} and an equivalent κ value of 7. The obtained OTFTs show high electric performance with carrier mobility of 0.20 cm^2 V^{-1} s^{-1}, on/off ratio of 4×10^5, threshold voltage of −0.6 V, and subthreshold slope of 0.7 V dec^{-1} when operated at −5 V. The results demonstrate the organometallic lanthanide complex is a promising candidate as gate insulator for low-voltage OTFTs.

1. Introduction

Organic thin-film transistors (OTFTs) have emerged as a vibrant field of research during the past decades in wearable and flexible electronics owing to their superiorities of flexibility, low-cost, and easy to fabrication in large-area [1–8]. To meet the rapid development of portable and miniaturization of various electronic devices such as sensors, radio-frequency identification (RFID) tags, and flat panel displayers, etc., great efforts have been devoted to reducing the power consumption of OTFTs [9–12]. Commonly, lower power consumption can be achieved by decreasing the operating voltages through employing high capacitance density of the gate dielectric (C_i), which can be addressed by means of either increasing the dielectric constant (κ) or/and decreasing the thickness of insulator [13,14]. In general, the high-κ dielectric materials, inorganic metal-oxides, need complicated processing routes such as radio-frequency magnetron sputtering, atomic layer deposition, and chemical vapor deposition, which are often associated with high temperature, cost, high-vacuum equipment [15–17]. It is reported that utilizing self-assembled monolayer or thin polymer film as insulators can induce a high charge carrier density at the conducting channel under a low gate voltage [18–20]. However, because of the low-κ of polymer dielectrics, the thickness of dielectrics should be drastically reduced (typically <10 nm) to achieve high capacitance. This demands a particular care in processing, since a very small amount of defects can cause a high leakage current, which is unacceptable for OTFTs [21–23]. To achieve low-voltage, high-performance OTFTs, design and preparation of gate insulating materials, especially organic high-κ dielectric materials with excellent dielectric properties and simple film forming is a long-term goal in material science [24,25].

The neutral molecule-based chirality organometallic lanthanide complexes, $Ln(tta)_3L_{2NR}$ (Ln = Eu^{3+}, Tb^{3+}, etc., tta = 2-thenoyltrifluoroacetonate, L_{2NR} = (−)-4,5-pinene bipyridine), have been proved to be promising candidates as gate dielectric materials, especially for the low operating voltage OTFTs owning to their good thermal stability, high-κ at room-temperature, easy film formation by thermal evaporation method [26]. In our recent work, we proposed $Eu(tta)_3L_{2NR}$ as dielectric layer to fabricate the low-voltage OTFTs [27]. However, this device was made by only specific lanthanide complex, which makes it not common enough, and also the fabrication and performance of devices remain challenging.

Here in this paper, we report a new high-κ organometallic lanthanide complex, $Tb(tta)_3L_{2NR}$, as gate dielectric, to fabricate low-voltage OTFTs. The thickness of $Tb(tta)_3L_{2NR}$ can be further reduced to 50 nm and using the polyvinyl alcohol (PVA) and octadecyltrichlorosilane (OTS) as modified layer. The as-obtained dielectric gate insulator showed superior properties of low leakage current density (~10^{-7} A cm^{-2}), low surface roughness (RMS of ca. 0.40 nm), and high-κ of 7. Furthermore, the OTFTs exhibited excellent electrical performance such as the mobility (μ) of 0.20 cm^2 V^{-1} s^{-1}, threshold voltage (V_{th}) of −0.6 V, on/off ratio of 4×10^5, and subthreshold slope (SS) of 0.7 V dec^{-1}. This indicates high-κ organometallic lanthanide

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complex has the potential applications as gate dielectric for low-voltage, high-performance OTFTs.

2. Experimental section

The similar technique was employed to synthesis $Tb(tta)_3L_{2NR}$, as described in the previous paper [26]. PVA with 80% hydrolysis level and ca. 10,000 weight-average molar mass is used as water-soluble modifier. OTS and pentacene are 95% and 99% in purity, respectively. All raw materials were purchased from Aldrich and used without further purification. Pentacene-based OTFTs had a bottom-gate top-contact architecture (Fig. 1) [28]. The glass substrate was cleaned and placed in the chamber. 50 nm Au strip was firstly deposited as gate electrode. And then, 50 nm $Tb(tta)_3L_{2NR}$ was deposited by thermal evaporation at about 150 °C. Subsequently, 4 mg ml^{-1} of PVA was dissolved in deionized water and spin-coated. This modification can significantly reduce the surface roughness of $Tb(tta)_3L_{2NR}$ film. The substrate was then placed onto a hotplate at 50 °C. Moreover, OTS monolayer was modified by vacuum vapor diffusion method. Namely, the as-prepared $Tb(tta)_3L_{2NR}$/PVA/OTS gate insulator has a triple-laminated structure. Pentacene films with 50 nm, patterned through a shadow mask, were deposited by vacuum deposition under a deposition pressure of 10^{-4} Pa at the same rate of 0.02 nm s^{-1}. Substrate temperature was chosen as 60 °C for pentacene films. Finally, 50 nm Au source-drain electrodes were deposited on the pentacene films by thermal evaporation through another mask. The channel length (L) and width (W) are 50 and 500 μm. As contrast, the OTFTs with $Tb(tta)_3L_{2NR}$, $Tb(tta)_3L_{2NR}$/PVA and heavily doped n-type (100) Si substrate with a 300 nm SiO_2 layer as gate insulator were also fabricated. In order to measure the leakage current and capacitive characteristic, a metal-insulator-metal (MIM) structure device was fabricated by deposition of 50 nm Au square with side of 150 μm onto the gate insulator.

Atomic force microscopy (AFM) images were obtained using Benyuan Nano-Instruments Ldt. CSPM5500 and X-ray diffraction (XRD) were determined by the Bruker D8 Advance A25, $K_{\alpha 1}$ = 1.78897 Å, Fe filter of 0.02 mm thickness. The electronic measurements were carried out in ambient atmosphere using a Keithley 4200-SCS semiconductor parameter analyzer.

3. Results and discussion

We first carried out the AFM investigations to reveal the morphological properties. The surfaces of $Tb(tta)_3L_{2NR}$, $Tb(tta)_3L_{2NR}$/PVA, and $Tb(tta)_3L_{2NR}$/PVA/OTS gradually reduced with a root-mean-square (RMS) roughness of 0.88, 0.56, and 0.40 nm, as shown in Fig. 2(a)–(c). The $Tb(tta)_3L_{2NR}$/PVA/OTS and SiO_2 (Fig. 2d, RMS of ca. 0.41 nm) exhibits the similar surface roughness, thus results in comparable morphology of the upper organic layers. PVA was used as water-soluble modifier, and then, OTS was deposited to transfer the hydrophilic hydroxyl groups to the hydrophobic surface, which is beneficial to enhance the electrical performance of the device [29]. Fig. 2(e)–(g) shows the morphologies of pentacene grains deposited onto $Tb(tta)_3L_{2NR}$, $Tb(tta)_3L_{2NR}$/PVA, and $Tb(tta)_3L_{2NR}$/PVA/OTS changing from dot-like shape to the common ridge-like shape. The pentacene films deposited on $Tb(tta)_3L_{2NR}$/PVA/OTS is observed similar morphology with pentacene on SiO_2, composed of highly structural ordering and large feature size (Fig. 2(h)). In addition, the pentacene layer on $Tb(tta)_3L_{2NR}$/PVA/OTS and SiO_2 dielectrics exhibits nearly identical surface roughness with an RMS value of 24.6 nm [30].

The XRD results validate the crystalline feature of the pentacene films, as shown in Fig. 2(i)–(l). The pentacene molecules were packed in the same structure on $Tb(tta)_3L_{2NR}$, $Tb(tta)_3L_{2NR}$/PVA, and $Tb(tta)_3L_{2NR}$/PVA/OTS, and the typical signals become better, which is in good agreement with the AFM measurements. The XRD patterns of pentacene films deposited on $Tb(tta)_3L_{2NR}$ and $Tb(tta)_3L_{2NR}$/PVA show weak peaks diffraction, suggesting the thin film phase of pentacene not yet fully formed (Fig. 2(i) and (j)). Similar crystallographic structures of pentacene deposited on both $Tb(tta)_3L_{2NR}$/PVA/OTS and SiO_2, which is indicated in Fig. 2(k) and (l). For the pentacene films, the (001) peaks are extracted from the XRD patterns, with the d value of 1.5 nm, suggesting the “thin film phase” of pentacene with herringbone stacking structure [31].

To show the feasibility of our fabricated thin film as gate dielectric for low-voltage, high-performance OTFTs, we fabricated an Au/insulator/Au (MIM) sandwiched structure and test its current-voltage and capacitance density-frequency characteristics. As shown in Fig. 3(a), with $Tb(tta)_3L_{2NR}$/PVA/OTS insulator layer, the leakage current density is as low as at the level of 10^{-7} A cm^{-2} at ± 5 V bias voltage, which suggests the low off current of OTFTs. Fig. 3(b) exhibits the frequency dependence of capacitance density and dielectric constant for the $Tb(tta)_3L_{2NR}$/PVA/OTS structure measured in the frequency of 10^2 to 10^6 Hz and bias voltage of 0 V. For the triple-laminated $Tb(tta)_3L_{2NR}$/PVA/OTS insulator, the total capacitance density is ca. 43 nF cm^{-2} at 10^2 Hz. When using the thickness value of ca. 150 nm, an equivalent κ value of about 7 can be extracted, which is far superior to 3.8 of SiO_2. Furthermore, the dielectric loss is lower than 0.1 in the range of the measurement frequency from 10^2 to 10^6 Hz.

Typical output and transfer characteristics of pentacene-based OTFTs using the $Tb(tta)_3L_{2NR}$, $Tb(tta)_3L_{2NR}$/PVA, $Tb(tta)_3L_{2NR}$/PVA/OTS and 300 nm SiO_2 as the gate insulators are shown in Fig. 4. Fig. 4(a)–(c) demonstrated the output curves of a representative p-type field effect behavior with clear linear and saturation regions. In the transfer curve of $Tb(tta)_3L_{2NR}$ insulator, the off current is as high as -5×10^{-11} A and on/off current ratio is only 10^2, which suggests the high leakage current (Fig. 4(e)). To $Tb(tta)_3L_{2NR}$/PVA insulator, the off current is as high as -8×10^{-11} A and on/off current ratio is about 10^3, which indicates PVA modification can obviously reduce the leakage current and improve the device performance (Fig. 4(f)). It is clearly seen that their electrical performances are distinctly inferior to those of pentacene-based OTFTs based on the $Tb(tta)_3L_{2NR}$/PVA/OTS as gate insulator, indicating that the OTS modification can further enhance the electrical performance. Due to the high capacitance of our $Tb(tta)_3L_{2NR}$/PVA/OTS system, the device can work effectively at operation voltages as low as -5 V, and by using a linear fit of the plot in the saturation region, the mobility of pentacene-based OTFTs can extract (Fig. 4(g)). Given the C_i value of

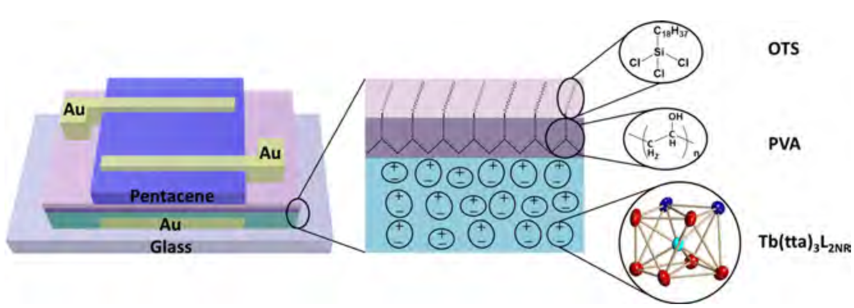

Fig. 1. Schematic diagram of a bottom-gate top-contact OTFTs using pentacene as the channel material and a triple-laminated configuration of $Tb(tta)_3L_{2NR}$/PVA/OTS as gate insulator.

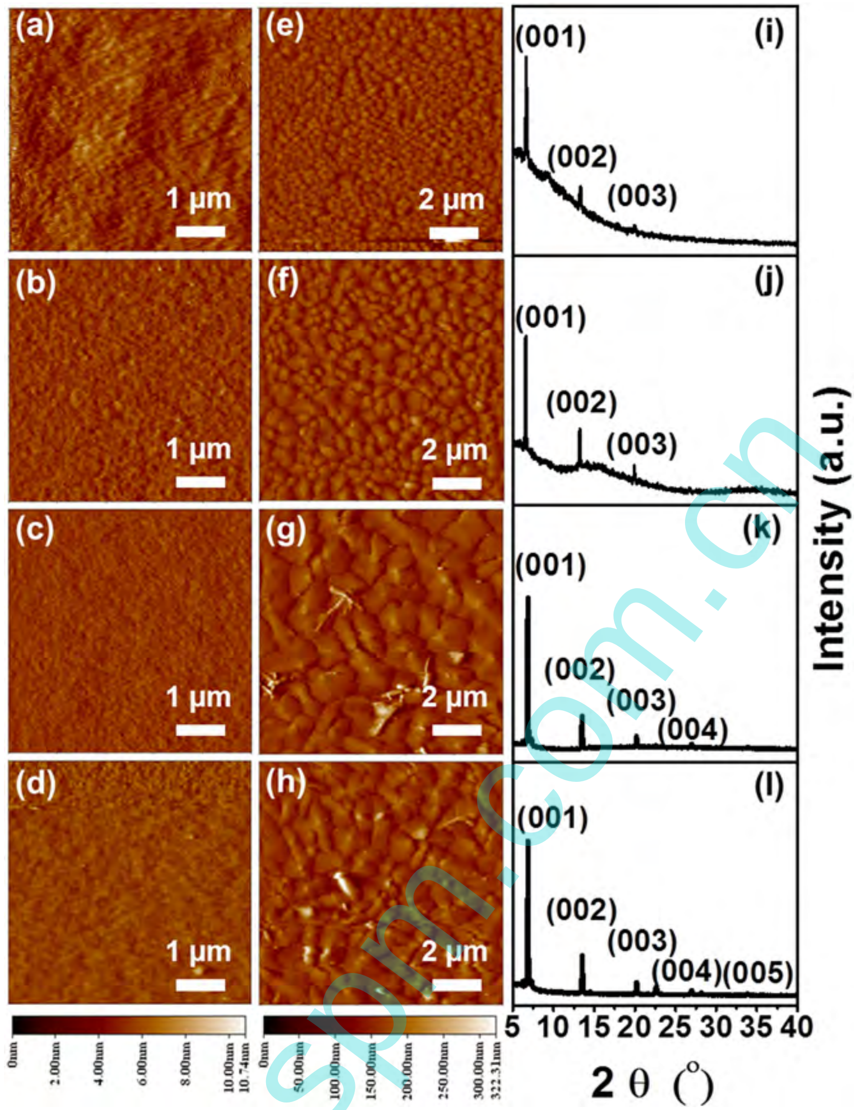

Fig. 2. The surface morphology and crystal structure of gate insulators and pentacene thin films. (a–d) AFM images of $Tb(tta)_3L_{2NR}$, $Tb(tta)_3L_{2NR}$/PVA, $Tb(tta)_3L_{2NR}$/PVA/OTS and SiO_2 as gate insulators. (e–h) AFM images of pentacene films deposited on the corresponding insulators of a–d. (i–l) The XRD patterns of pentacene films of e–h.

the $Tb(tta)_3L_{2NR}$/PVA/OTS system under zero bias of 43 nF cm^{-2} at 10^2 Hz, the mobility (μ) was calculated to be around 0.20 $cm^2\,V^{-1}\,s^{-1}$ with a high on/off ratio of 4×10^5, a low threshold voltage (V_{th}) of −0.6 V, and a low subthreshold slope (SS) of 0.7 V dec^{-1}. In addition, the off current is as low as 10^{-12} A, which means the low leakage current. Moreover, because SS is the indicators for estimating the charge trap density at the organic/insulator interface, the value of estimated maximum trap density (N_{trap}) is ca. 1.1×10^{12} cm^{-2} for $Tb(tta)_3L_{2NR}$/PVA/OTS insulator [32]. The properties of the low-voltage pentacene TFTs using $Tb(tta)_3L_{2NR}$/PVA/OTS as the gate dielectric are better than those prepared on various high-κ metal-oxide thin films, such as Al_2O_3 [15], Gd_2O_3 [33],

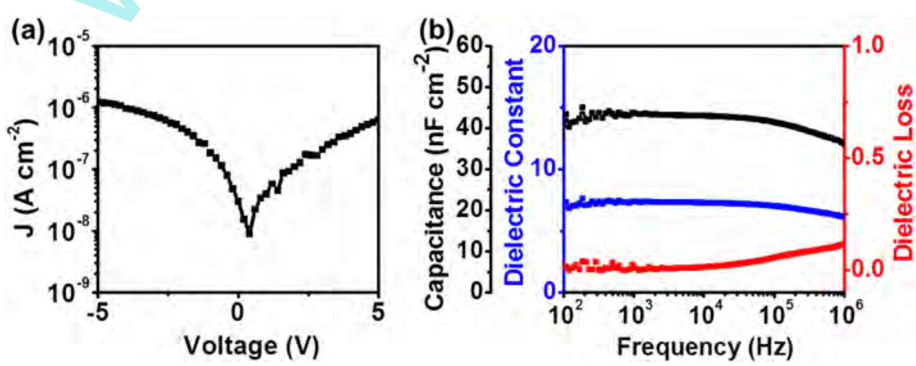

Fig. 3. The electrical characteristics of $Tb(tta)_3L_{2NR}$/PVA/OTS thin film. (a) Plot of leakage current density versus bias voltage of the MIM device. (b) The relationship of dielectric capacitance density, dielectric constant and dielectric loss versus frequency, measured at 0 V bias voltage.

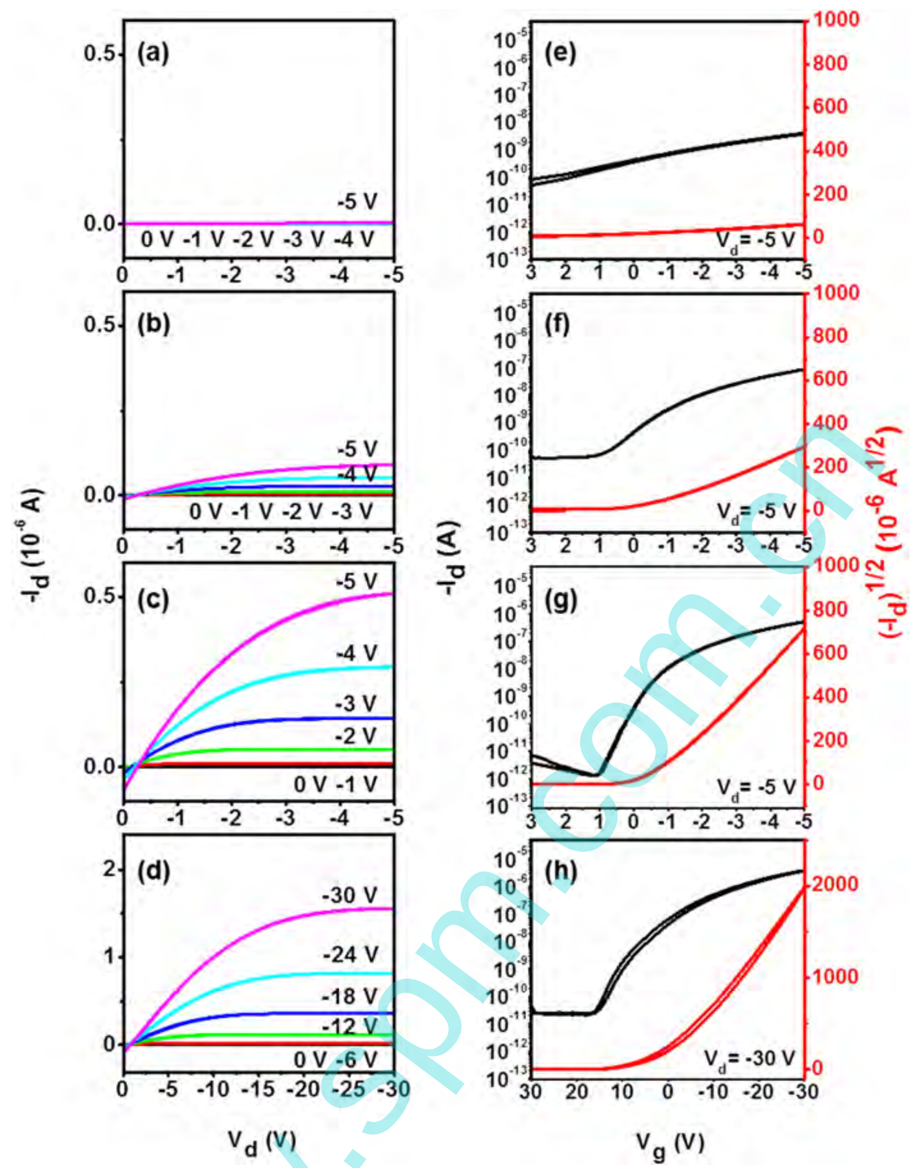

Fig. 4. (a–d) Output curves, (e–h) Transfer curves of OTFTs using the $Tb(tta)_3L_{2NR}$, $Tb(tta)_3L_{2NR}$/PVA, $Tb(tta)_3L_{2NR}$/PVA/OTS and 300 nm SiO_2 as dielectric at a constant V_d of −5 V and −30 V, respectively.

Ta_2O_5 [34], and even higher than the value reported by ultrathin polymers as gate dielectrics [35].

To further exhibit the superior electrical performances of high-κ $Tb(tta)_3L_{2NR}$/PVA/OTS thin films, we also deliberately fabricated pentacene-based OTFTs with a 300 nm SiO_2 as the gate insulator. Fig. 4(d) shows the output characteristics with a high gate voltage of −30 V. As shown in transfer curves of Fig. 4(h), the μ, on/off ratio, V_{th}, and SS correspond to 0.13 $cm^2\ V^{-1}\ s^{-1}$, 8 × 10^5, −1.0 V, and 2.9 V dec^{-1}. And N_{trap} is calculated to ca. 3.5 × 10^{12} cm^{-2}, which is three times as high as that of $Tb(tta)_3L_{2NR}$/PVA/OTS-based OTFTs.

4. Conclusion

In summary, we have achieved low-voltage OTFTs by introducing a high-κ triple-laminated thin film of $Tb(tta)_3L_{2NR}$/PVA/OTS as the gate insulator. The triple-laminated thin film exhibits a very smooth surface with RMS of about 0.40 nm, a low leakage current density of 10^{-7} A cm^{-2}, a high capacitance of 43 nF cm^{-2} and an equivalent κ value of 7. The corresponding pentacene-based OTFTs show good μ of 0.20 $cm^2\ V^{-1}\ s^{-1}$, V_{th} of −0.6 V and SS value of only 0.7 V dec^{-1} under an operation voltage as low as −5 V, and this performance is much better than that of the analogue devices obtained on conventional 300 nm SiO_2 substrates as insulator operated at −30 V (0.13 $cm^2\ V^{-1}\ s^{-1}$, −1.0 V and 2.9 V dec^{-1} for mobility, V_{th} and SS value, respectively). Our low-temperature method for fabrication of high-κ gate dielectric demonstrates significantly approach to realize low-voltage circuits.

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